

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Moriyoshi NAKASHIMA et al.

Filing Date: April 18, 2006

For: SEMICONDUCTOR CHIP MOUNTED INTERPOSER,
SEMICONDUCTOR DEVICE, SEMICONDUCTOR CHIP INTERPOSER
FABRICATION METHOD, BARE CHIP MOUNTED INTERPOSER, AND
INTERPOSER SHEET

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

**Mail Stop PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

PRELIMINARY AMENDMENT

Sir:

Entry of the following amendments prior to calculation of the filing fee and
examination is respectfully requested.